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# Theoretical and Experimental Investigation of a Balanced Phase-Locked Loop Based Clock Recovery at a Bit Rate of 160 Gb/s

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## Introduction

In high-speed Optical Time Division Multiplexed (OTDM) transmission systems, pre-scaled clock recovery (CR) is essential. This may be performed using e.g. opto-electronic phase-locked loops (OPLL) [1]. The highest data rates that a pre-scaled base rate clock has been extracted from so far are achieved with OPLLs (400 Gb/s) [1]. Recently, OPLLs with balanced photodetection, offering much simpler electronic processing and feedback, have been suggested and experimentally demonstrated [2-3]. So far, though, a comprehensive theoretical frame of description of this balanced loop has been missing. In this paper, a mathematical model of a balanced OPLL is described and key parameters are derived. Particularly the lock-in time, which is required to be very fast for some network applications, is investigated in terms of clock pulse width, loop filter gain and residuals of the balancing DC level. Based on the guidelines from the theoretical evaluations, a very simple experimental demonstration including a single electroabsorption modulator as phase comparator is constructed.

## Model Set-up

The model set-up for the balanced OPLL based CR is shown in Figure 1. Based on this model, a general non-linear differential equation (NDE) is derived. This NDE defines the evolution of the total phase error in the loop and its solutions reveal the dynamics of the balanced PLL.

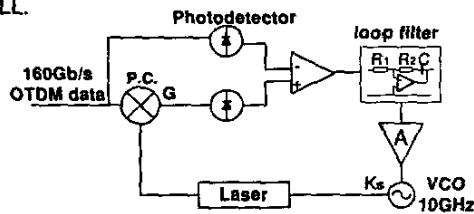


Figure 1. Schematic set-up.

The phase comparator (P.C.) mixes the optical OTDM data signal (160 Gb/s) with the locally generated optical clock signal at the base rate (10 GHz), producing an error signal. The mixing process corresponds to a mathematical multiplication with a mixer gain  $G$ . In practise non-linear processes like FWM in SOAs can be used to achieve the mixing [1]. The error signal is an offset sinusoidal with frequency  $\Delta f$ , given by the difference between the 16<sup>th</sup> frequency component of the clock signal and the line rate of the data. The amplitude of the error signal is  $s_1 c_{16}$ , which is a product

between the 1<sup>st</sup> and 16<sup>th</sup> Fourier frequency component of the corresponding data and clock signal. The balanced photodetection (BW 100 MHz) provides the subtraction of the DC level from the error signal, which results in a bipolar error signal. This subtraction also helps to stabilise the error signal against fluctuations in the input powers. The signal is then low pass filtered and fed back to the VCO, which controls the optical clock generating laser. The data signal is a 160 Gb/s PRBS modulated ( $2^8-1$ ) pulse train (FWHM 2.5 ps) with the average power of 15 dBm. The FWHM of the clock signal pulses  $T^{clk}$  is varied between: 0.5ps, 1ps, 2ps, 3ps and 8ps. The average power of the clock signal is also 15dBm.

## First Order Loop

The first order loop does not include the loop filter and therefore the dynamics are easier to understand. We are interested in determining under which conditions the loop locks and the corresponding lock-in time. In Figure 2(a) the minimum value of  $K$ , needed to obtain the lock, is plotted as a function of  $\Delta f$ .  $K$  is a product between the gain of the amplifier,  $A$ , and the sensitivity of the VCO,  $K_s$ . For convenience  $G$  is set to unity.

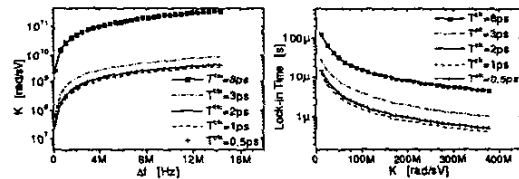


Figure 2. (a) Minimum value of  $K$  in order to obtain locking. (b) Lock-in time as function of  $K$ .

The lowest values of  $K$  are obtained when the clock FWHM is 1ps, while the largest values of  $K$  are obtained when the FWHM is 8ps. Even though the values of  $K$  seem large, they are easily attainable with standard commercial electronic components. In Figure 2(b) the lock-in time is plotted as a function of  $K$ . The frequency difference  $\Delta f$  is assumed to be 0. The lock-in time is minimized when the FWHM of the clock signal is 1ps. Based on [4], the lock-in time,  $T$ , for small initial phase differences, ( $<\pi/4$ ) is approximated to

$$T = \frac{2.19}{\left[ 2 \cdot 16 \cdot R \cdot K \cdot s_1 \cdot c_{16} \sqrt{1 - \left( \frac{2 \cdot \pi \cdot \Delta f}{2 \cdot 16 \cdot R \cdot K \cdot s_1 \cdot c_{16}} \right)^2} \right]} \quad (1)$$

where  $R$  is the responsivity of the photodiode. Equation (1) shows how a maximized  $c_{16}$  results in a minimized lock-in time and reveals the importance of a large error

signal. For the specified set-up,  $c_{16}$  is maximized for a FWHM of 1ps, confirming the results shown in Figure 2(b).

### Second Order Loop

Now the loop filter is implemented. In many cases the loop filter is a Proportional Integrator (PI). Even though the balanced photodetection provides a subtraction of the DC level, the DC level might not be fully subtracted due to imperfections in the electronics. If the compensated DC level is constant and fulfils the following relation,  $DC \leq 2s_1 c_{16}$ , the loop locks.

The impact on the lock-in time of the uncompensated DC level, defined as the ratio between the DC level after compensation divided by the DC level before compensation, is shown in Figure 3.

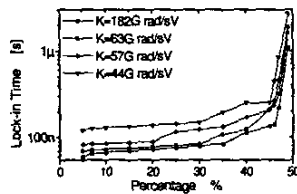


Figure 3. Lock-in time as a function of the uncompensated level in the error signal.

If the uncompensated DC  $\leq 45\%$ , the influence on the lock-in time is negligible. For practical circuits this level of compensation can be fulfilled.

Next the lock-in time is plotted as a function of K for increasing  $\Delta f$ . In Figure 4(a) the FWHM of the clock signal pulses is 1ps corresponding to the optimum FWHM for the first order loop.

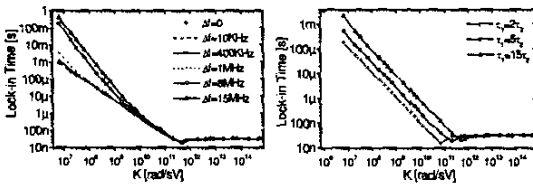


Figure 4. (a) Lock-in time as a function of K for increasing  $\Delta f$ . (b) Lock-in time for different ratios of the filter's time constants.

For small values of K the lock-in time increases as the frequency detuning increases. When K exceeds  $2 \cdot 10^{11}$  rad/sV, the lock-in time becomes constant (for  $\Delta f$  up to 15 MHz). The lowest value of the lock-in time is 25ns.

Figure 4(b) shows how the lock-in time changes as the ratio between the time constants of the PI filter; i.e.  $\tau_1$  and  $\tau_2$  is changed ( $\tau_1/\tau_2 = R_1 C / R_2 C = R_1 / R_2$ ). The bandwidth of the filter is constant. For large values of K the lock-in time approaches the same value irrespective of the ratio. However, the minimum value of the lock-in time (15ns) is obtained when  $\tau_1/\tau_2 = 2$ . For low values of K, the lowest lock-in times remain for  $\tau_1/\tau_2 = 2$ . This is because the gain of the PI filter increases as  $R_1/R_2$  decreases.

### Experimental Demonstration

A simple manifestation of the CR circuit based on the balanced OPLL is implemented at 160 Gb/s. The phase comparator is an electroabsorption modulator (EAM) and the FWHM of the switching windows, which corresponds to  $T^{clk}$ , is 8ps. The EAM is driven electrically instead of through a laser, and the scheme works well. The CR unit locks to a 160 Gb/s data stream and remains stable. The frequency power spectrum of the recovered 10 GHz clock and its single sideband phase noise are shown in Figure 5, yielding a narrow peak with very low timing jitter (323 fs).

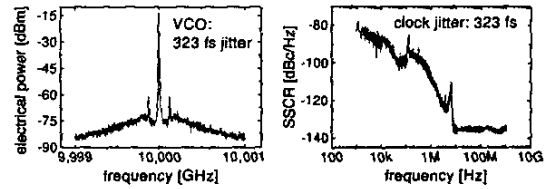


Figure 5. (a) Frequency spectrum of the recovered clock. (b) Single sideband to carrier ratio (SSCR) revealing a timing jitter of 323 fs.

The value of K is above the required value determined by Figure 2(a). Also the DC level is subtracted sufficiently, minimizing the influence on the PLL operation. The performance of this CR unit is sufficient for a 160 Gb/s demultiplexer/receiver, but by using the proposed model it is expected that the performance can be further improved.

### Conclusion

A detailed model of the balanced OPLL has been presented. It was shown how the lock-in time can be minimized by optimising  $T^{clk}$  (1ps), carefully compensate the DC level ( $<45\%$ ), use sufficiently high loop gain ( $K > 10^{11}$ ) and match the time constants of the loop filter ( $\tau_1/\tau_2 = 2$ ). Furthermore, a successful experimental implementation of the scheme was demonstrated. We believe the model to be a powerful tool for designing CR circuits based on the OPLL technique.

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